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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,434	02/06/2004	Ramachandran Krishnaswamy	333772000800	5995

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EXAMINER
LO, SUZANNE

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/772,434	KRISHNASWAMY ET AL.
	Examiner	Art Unit
	Suzanne Lo	2128

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _06 February 2004_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-23_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _06 February 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _9/7/04 9/27/04 9/20_

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-23 have been presented for examination.

PRIORITY

2.   Acknowledgment is made of applicant's claim for priority to provisional application 60/447839

filed on 02/14/03 and to provisional application 60/449622 filed on 02/24/03.

Information Disclosure Statement

3.   The information disclosure statements (IDS) submitted on 09/07/04, 09/27/04, 09/20/05, and

03/10/06 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has

considered the IDS' as to the merits.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition
of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
conditions and requirements of this title.

4.   Claims 1-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-

statutory subject matter. Specifically, claims 1-23 do not produce a tangible result. The claims do not

enable their usefulness to be realized, there is only specifying and describing being performed and there is

no tangible output. The software constructs exist only in a processor and do not allow their usefulness to

be realized in a tangible form.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and
process of making and using it, in such full, clear, concise, and exact terms as to enable any
person skilled in the art to which it pertains, or with which it is most nearly connected, to make

and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5.   Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The aforementioned claim is an improper dependent claim – it is dependent on self and not further limiting.

Claim 18 is not treated on merit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis

for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   **Claims 1-3, 5-6, 9-10, 16, 19-23 are rejected under 35 U.S.C. 102(e) as being clearly anticipated**

by Hollander (U.S. Patent Application Publication 2002/0073375 A1).

As per claim 1, Hollander is directed to a method for developing a test program in general

purpose C/C++ constructs, the test program for testing a semiconductor integrated circuit (IC) in a

semiconductor test system ([0040]-[0041]), the method comprising: describing test system resources, test

system configuration, and module configuration in general-purpose C/C++ constructs for the

development of a test program to test the IC on the semiconductor test system ([0035], [0042]);

describing a test sequence in general-purpose C/C++ constructs for the development of the test program

to test the IC on the semiconductor test system ([0043]); describing a test plan in general-purpose C/C++

constructs for the development of the test program to test the IC on the semiconductor test system

([0044]); describing test conditions in general-purpose C/C++ constructs for the development of the test

program to test the IC on the semiconductor test system ([0045]); describing test patterns in general-

purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test

system ([0068]); and describing timing of the test patterns in general-purpose C/C++ constructs for the

development of the test program to test the IC on the semiconductor test system ([0060], [0068], [0085]).

As per claim 2, Hollander is directed to the method of claim 1, wherein describing test system

resources comprises: specifying a resource type, wherein the resource type is associated with at least one

test module for applying a test to the IC; specifying a parameter type associated with the resource type,

and specifying a parameter of the parameter type ([0068]-[0070]).

As per claim 3, Hollander is directed to the method of claim 1, wherein describing test system

configuration comprises: specifying a site controller for controlling at least one test module, each test

module for applying a test to the IC; and specifying an input port of a module connection enabler,

wherein the test system couples the site controller to the module connection enabler at the input port, and

the module connection enabler couples the site controller to the at least one test module (**Figure 1, test**

files 12, 20 and drive 32).

As per claim 5, Hollander is directed to the method of claim 1, wherein describing module

configuration comprises: specifying a module identifier for specifying a module type ([0074]-[0076]);

specifying executable code for controlling a test module of the module type specified by the module

identifer, the test module for applying a test to the IC ([0074]-[0076]); and specifying a resource type

associated with the test module ([0068]-[0070]).

As per claim 6, Hollander is directed to the method of claim 5, the method further comprising

specifying a slot identifier for specifying an output port of a module connection enabler, wherein the test

system couples the test module to the module connection enabler at the output port, and the module

connection enabler couples the test module to a corresponding site controller ([0074]-[0076]).

As per claim 9, Hollander is directed to the method of claim 5, further comprising specifying a

vendor identifier for identifying the provider of the test module (Figure 3).

As per claim 10, Hollander is directed to the method of claim 5, further comprising specifying an

identifier of the maximum number of resource units available in connection with the resource type

(Figure 3).

As per claim 16, Hollander is directed to the method of claim 5, wherein the resource type is

arbitrary waveform generation pins and the resource units are tester channels ([0095], Figure 1, Drive 32,

test generator 26).

Claim 18 not treated on merit.

As per claim 19, Hollander is directed to the method of claim 1, wherein describing test

conditions comprises: specifying at least one test condition group (Figure 1, test files 20 and Figure 2,

test files 205).

As per claim 20, Hollander is directed to the method of claim 19, wherein describing test

conditions further comprises: specifying at least one specification set including at least one variable; and

specifying a selector for selecting an expression to be bound to a variable (Figure 1, test files 20 and

Figure 2, test files 205).

As per claim 21, Hollander is directed to the method of claim 20, wherein association of the test

condition group with a selector for the at least one specification set defines a test condition (Figure 1, test

files 20 and Figure 2, test files 205).

As per claim 22, Hollander is directed to the method of claim 21, wherein the test condition is an

object (Figure 1, test files 20 and Figure 2, test files 205).

As per claim 23, Hollander is directed to the method of claim 1, wherein describing a test

sequence comprises specifying: a result of executing a flow or test; an action based upon the result; and a

transition to another flow or test based upon the result **(Figure 1, module 24)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be
> patented and the prior art are such that the subject matter as a whole would have been obvious at
> the time the invention was made to a person having ordinary skill in the art to which said subject
> matter pertains. Patentability shall not be negatived by the manner in which the invention was
> made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966),

that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are

summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or
   nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under
35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly
owned at the time any inventions covered therein were made absent any evidence to the contrary.
Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of
each claim that was not commonly owned at the time a later invention was made in order for the examiner
to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under
35 U.S.C. 103(a).

7.   **Claims 8 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander**

(U.S. Patent Application Publication 2002/0073375 A1).

As per claim 8, although Hollander does not specifically disclose the method of claim 5, wherein the executable code is a dynamic link library, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to minimize memory usage.

As per claim 11, although Hollander does not specifically disclose the method of claim 5, wherein the resource type is digital tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals ([0095]) and resource units as tester channels (**Figure 1, drive 32, test generator 26**) so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 12, although Hollander does not specifically disclose the method of claim 5, wherein the resource type is analog tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals ([0095]) and resource units as tester channels (**Figure 1, drive 32, test generator 26**) so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 13, although Hollander does not specifically disclose the method of claim 5, wherein the resource type is RF tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals ([0095]) and resource units as tester channels (**Figure 1, drive 32, test generator 26**) so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 14, although Hollander does not specifically disclose the method of claim 5, wherein the resource type is power supply pins and the resource units are tester channels, Hollander discloses driving any simulator signals ([0095]) and resource units as tester channels (**Figure 1, drive 32, test generator 26**) so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 15, although Hollander does not specifically disclose the method of claim 5, wherein the resource type is digitizer pins and the resource units are tester channels, Hollander discloses driving any simulator signals ([0095]) and resource units as tester channels (**Figure 1, drive 32, test generator 26**) so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

8.   Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hollander (U.S. Patent Application Publication 2002/0073375 A1) in view of National Instruments ("Matrix Switch Expansion Guide").**

As per claim 4, Hollander is directed to the method of claim 3, but fails to specifically disclose wherein the module connection enabler is a switch matrix. National Instruments teaches a switch matrix as a connection enabler for unit under test (**page 1, 1st paragraph**). Hollander and National Instruments are analogous art because they are both from the same field of endeavor, testing circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the test program of Hollander with the switch matrix of National Instruments in order to eliminate the need to duplicate instruments and reduce the cost to test (**page 1, 1st paragraph**).

As per claim 7, Hollander is directed to the method of claim 6, but fails to specifically disclose wherein the module connection enabler is a switch matrix. National Instruments teaches a switch matrix as a connection enabler for unit under test (**page 1, 1st paragraph**). Hollander and National Instruments are analogous art because they are both from the same field of endeavor, testing circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the test program of Hollander with the switch matrix of National Instruments in order to eliminate the need to duplicate instruments and reduce the cost to test (**page 1, 1st paragraph**).

9.   Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hollander (U.S. Patent**

Application Publication 2002/0073375 A1) in view of Schauss et al. (U.S. Patent No. 5,181,201).

As per claim 17, Hollander is directed to the method of claim 5, but fails to specifically disclose

wherein the resource type is associated with resource units, the method further comprising specifying an

indicator relating to which resource units are disabled. Schauss teaches an indicator for disabled resource

units (**Schauss, column 13, lines 54-62**). Hollander and Schauss are analogous art because they are both

from the same field of endeavor, interfacing chip devices. It would have been obvious to one of ordinary

skill in the art at the time of the invention to combine the test program of Hollander with the disabled

indicator of Schauss in order to track non-operational inputs (**Schauss, column 13, lines 54-62**).

Conclusion

10.   The prior art made of record is not relied upon because it is cumulative to the applied rejection.

These references include:

    1. U.S Patent No. 5,488,573 issued to Brown et al. on 01/30/96.

    2. U.S. Patent No. 6,195,774 B1 issued to Jacobson on 02/27/01.

11.   All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be
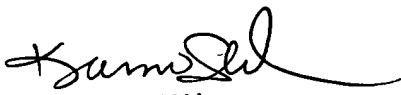
reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this

application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

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CANADA) or 571-272-1000.

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
07/06/06

KAMINI SHAH
SUPERVISORY PATENT EXAMINER